

Claims

- [c1] 1. A method of operating a control chip having a multiple-layer defer queue between a first bus and a second bus, the method comprising: storing a request in the multiple-layer defer queue, wherein the request is issued by the first bus; issuing a defer response or a retry response with respect to the request to the first bus; issuing the request to the second bus; receiving a responded data with respect to the request from the second bus; providing the responded data to the first bus if the defer response issues to the first bus; and providing the responded data to the first bus if the retry response issues to the first bus and only when the first bus again issues the request.
- [c2] 2. The method of claim 1, wherein in the step of storing the request into the multiple-layer defer queue, the multiple-layer defer queue also provides a request record with respect to the request.
- [c3] 3. The method of claim 2, wherein after the step of providing the responded data to the first bus, the corresponding request and the corresponding request record in the multiple-layer defer queue are deleted.
- [c4] 4. The method of claim 2, wherein the request record comprises: an identification code field, used to store an identification code with respect to the request; a flag field, used to judge whether the request is one selected from the group consisting of the retry response and the defer response; and an effective data field, used to enable the effective data field when the responded data is received.
- [c5] 5. The method of claim 4, wherein when the first bus again issues the request, an effective bit of the effective data field should be checked to be an enable status, then the responded data is sent to the first bus.
- [c6] 6. The method of claim 1, wherein the request includes one selected from the group consisting of an input/output (I/O) read request, an I/O write request, and a memory read request.
- [c7] 7. A method of operating a control chip having a multiple-layer defer queue between a first bus and a second bus, the method comprising: storing a plurality

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from the CPU bus, and generating a PCI request record; a multi-layer defer queue, when receiving the CPU request, respectively responding to the CPU bus by one of a defer response and a retry response; a PCI access queue, receiving the PCI request record; and a PCI controller, receiving the request from the multi-layer defer queue, causing the PCI request record of the PCI access queue to be transmitted to the PCI bus via the PCI controller; wherein when the PCI bus generates a response data and if the CPU request in the multi-layer defer queue is to produce the defer response, then the response data is directly sent to CPU bus, if the CPU request in the multi-layer defer queue is to produce the retry response and the CPU bus issues the CPU request, then the response data is transmitted to the CPU bus.